IN THE CLAIMS

Please amend the claims as follows:

67. (Previously Presented) An image system comprising:

a one-dimensional array of image sensors configured to photoelectrically convert an optical image into an electrical signal corresponding to a light amount of the optical image in units of the image sensors, each of the image sensors comprising a photoelectric converter, an amplification transistor having a gate to which said photoelectric converter is connected through a transfer transistor and for amplifying an output signal from said photoelectric converter and outputting the electrical signal, a selection transistor having a gate to which a selection signal is supplied, and a reset transistor connected to a connection point between said amplification transistor and said transfer transistor;

noise cancellers, each of which is connected to an image sensor and subtracts a noise component from the electrical signal, each of the noise cancellers comprising a sample/hold capacitor to which the electrical signal from said image sensor is supplied through a clamp capacitor and a sample/hold transistor, and a clamp transistor connected to a connection point between said clamp capacitor and said sample/hold transistor; and

a semiconductor substrate including a p^--type impurity base layer and a p^+-type impurity layer formed thereon, and wherein said array of image sensors is formed in said p^+-type impurity layer.

68. (Previously Presented) The image system according to claim 67, further comprising an image monitor configured to display an image based on the electrical signal from said noise cancellers.

69. (Previously Presented) The image system according to claim 67, further comprising a printer configured to print an image based on the electrical signal from said noise cancellers.

70. (Previously Presented) The image system according to claim 67, wherein said selection transistor selectively turns on said amplification transistor.

71. (Previously Presented) The image system according to claim 67, wherein said reset transistor selectively resets the gate of said amplification transistor.

72. (Previously Presented) The image system according to claim 67, wherein said sample/hold capacitor comprises a first terminal connected to the sample/hold transistor and a second terminal connected to a ground potential.

73. (Withdrawn) The image system according to claim 67, wherein each of said noise cancellers further comprises a source follower circuit connected between said image sensor and said clamp capacitor.

74. (Withdrawn) The image system according to claim 67, wherein each of said noise cancellers further comprises a correction capacitor connected to a connection point between said image sensor and said clamp capacitor configured to decrease a difference between impedances of said clamp capacitor in ON and OFF periods.

75. (Canceled).

76. (Previously Presented) The image system according to claim 67, wherein said sample/hold capacitor and said clamp capacitor are stacked on each other.

77. (Previously Presented) The image system according to claim 67, wherein said image sensors are two-dimensionally arrayed.

78. (Previously Presented) An image system comprising:

a one-dimensional array of image sensors configured to photoelectrically convert an optical image into an electrical signal corresponding to a light amount of the optical image in units of the image sensors;

noise cancellers, each of which is connected to an image sensor and subtracts a noise component from the electrical signal, each of the noise cancellers comprising a sample/hold

capacitor to which the electrical signal from said image sensor is supplied through a sample/hold transistor and a clamp capacitor, and a clamp transistor connected to a connection point between said clamp capacitor and said sample/hold capacitor; and

a semiconductor substrate including a p^--type impurity base layer and a p^+-type impurity layer formed thereon, and wherein said array of image sensors is formed in said p^+-type impurity layer.

79. (Previously Presented) The image system according to claim 78, wherein said sample/hold capacitor comprises a first terminal connected to the clamp capacitor and a second terminal connected to a ground potential.

80. (Currently Amended) The image system according to claim 78, wherein each of said image sensors comprises:

a photoelectric converter;

an amplification transistor having a gate to which said photoelectric converter is connected and for amplifying an output signal output from said photoelectric converter and ~~output~~ outputting an amplified signal;

a selection transistor having a gate to which a selection signal is supplied; and

a reset transistor connected to a connection point between said amplification transistor and said selection transistor.

81. (Withdrawn) The image system according to claim 80, wherein said selection transistor selectively turns on said amplification transistor.

82. (Withdrawn) The image system according to claim 80, wherein said reset transistor is connected between the gate of the amplification transistor and the connection point between said amplification transistor and said selection transistor and selectively resets the gate of said amplification transistor.

83. (Withdrawn) The image system according to claim 80, wherein each of said image sensors further comprises a feedback capacitor connected between the reset transistor and the gate of said amplification transistor.

84. (Withdrawn) The image system according to claim 80, wherein each of said image sensors further comprises a discharge transistor connected between the gate of said amplification transistor and a gate of the reset transistor.

85. (Withdrawn) The image system according to claim 80, wherein each of said image sensors further comprises a transfer transistor connected between the gate of said amplification transistor and the photoelectric converter.

86. (Withdrawn) The image system according to claim 78, wherein each of said image sensors comprises:

photoelectric converters;

selection transistors respectively connected to said photoelectric converters and configured to select one of output signals from said photoelectric converters; and

an output circuit configured to receive one of the output signals from said photoelectric converters which is selected by said selection transistors, amplify the output signal, and output an amplified signal.

87. (Withdrawn) The image system according to claim 86, wherein said output circuit comprises:

an amplification transistor having a gate to which said selected one of the output signals from said photoelectric converters is supplied,

a selection transistor having a gate to which a selection signal is supplied, and

a reset transistor connected to said selection transistor.

88. (Withdrawn) The image system according to claim 86, wherein said selection transistor selectively turns on said amplification transistor.

89. (Withdrawn) The image system according to claim 86, wherein said reset transistor is connected between the gate of the amplification transistor and said selection transistor and selectively resets the gate of said amplification transistor.

90. (Withdrawn) The image system according to claim 86, wherein said output circuit comprises:

an amplification transistor having a gate to which said selected one of the output signals from said photoelectric converters is supplied,

a selection capacitor to which a selection signal is supplied, and

a reset transistor connected to said selection capacitor.

91. (Withdrawn) The image system according to claim 86, wherein said photoelectric converters are arranged side by side in a vertical direction.

92. (Withdrawn) The image system according to claim 86, wherein said photoelectric converters are arranged side by side in a horizontal direction.

93. (Withdrawn) The image system according to claim 92, wherein the output signals from said photoelectric converters are supplied to a first node of a reset transistor and a gate of the amplification transistor through the photodiode selection transistors.

94. (Withdrawn) The image system according to claim 78, wherein each of said image sensors comprises:

four photoelectric converters arranged in a 2×2 matrix;

selection transistors respectively connected to said photoelectric converters and configured to select one of output signals from said photoelectric converters; and

an output circuit configured to receive one of the output signals from said photoelectric converters which is selected by said selection transistors, amplify the output signal, and output an amplified signal.

95. (Withdrawn-Currently Amended) The image system according to claim 78, wherein each of said image sensors comprises:

a photodiode;

an amplification transistor having a gate to which the photodiode is connected and for amplifying an output signal output from said photoelectric converter and ~~output~~ outputting an amplified signal;

a reset transistor to which the photodiode is connected and for resetting a signal electric charge; and

an address capacitor connected between a first node and the gate of the amplification transistor.

96. (Withdrawn-Currently Amended) The image system according to claim 78, wherein each of said image sensors comprises:

a photodiode;

an amplification transistor having a gate to which the photodiode is connected and for amplifying an output signal from said photoelectric converter and ~~output~~ outputting an amplified signal; and

an address capacitor connected between a first node and the gate of the amplification transistor.

97. (Withdrawn-Currently Amended) The image system according to claim 96, wherein each of said image sensors further comprises a transmitting transistor connected between the photodiode and the gate of the amplification transistor ~~64~~.

98. (Withdrawn-Currently Amended) The image system according to claim 78, wherein each of said image sensors comprises:

a photodiode;

an amplification transistor having a gate to which the photodiode is connected and for amplifying an output signal output from said photoelectric converter and ~~output~~ outputting an amplified signal;

a transmitting transistor connected between the photodiode and the gate of the amplification transistor; and

a reset transistor connected to a connection point between said amplification transistor and said transmitting transistor.

99. (Withdrawn-Currently Amended) The image system according to claim 78, wherein each of said image sensors comprises:

a photodiode;

an amplification transistor having a gate to which the photodiode is connected and for amplifying an output signal from said photoelectric converter and ~~output~~ outputting an amplified signal;

an address capacitor connected between a first node and the gate of the amplification transistor; and

a transmitting transistor connected between the photodiode and the gate of the amplification transistor.

100. (Withdrawn) The image system according to claim 78, wherein each of said noise cancellers further comprises a source follower circuit connected between said image sensor and said clamp capacitor.

101. (Withdrawn) The image system according to claim 78, wherein each of said noise cancellers further comprises a correction capacitor connected to a connection point between said image sensor and said clamp capacitor configured to decrease a difference between impedances of said clamp capacitor in ON and OFF periods.

102. (Canceled)

103. (Withdrawn) The image system according to claim 78, wherein said sample/hold capacitor and said clamp capacitor are stacked on each other.

104. (Withdrawn) The image system according to claim 78, wherein said image sensors are two-dimensionally arrayed.